IN THE UNITED STATES PAT	TENT AND TRADEMARK OFFICE
In Re Patent Application of:	)
Nick Lindert et al.	Examiner: Nguyen, Joseph H.
Application No.: 10/816,311	) Art Unit: 2815
Filed: March 31, 2004	)
For: BULK NON-PLANAR TRANSISTOR HAVING STRAINED ENHANCED MOBILITYY AND METHODS OF FABRICATION	) ) ) )
Commissioner for Patents P.O. Box 1450 Alexandria, Virginia, 22313-1450	

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If	there ar	e any ac	dditional charges, please charge Deposit Account No. 02-2666.
			Respectfully submitted,
			BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
Dated: Z	/11	_, 2005	Michael A. Bernadicou 35,934

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	×				Examiner Name	Nguyen, Joseph
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## Complete if Known Substitute for Form 1449/PTO **Application Number** 10/816,311 INFORMATION DISCLOSURE Filing Date 3/31/2003 STATEMENT BY APPLICANT First Named Inventor: Nick Lindert (use as many sheets as necessary) Art Unit 2815 **Examiner Name** Nguyen, Joseph 42P18257 2 2 **Attorney Docket Number** 42P18257 Sheet NON PATENT LITERATURE DOCUMENTS $\mathsf{T}^2$ Cite Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the Examiner No<sup>1</sup> Initials\* item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published T. Park et al., "Fabrication of Body-Tied FinFETs (Omega MOSFETS) Using Bulk Si Wafers", 2003 Symposia on VLSI Technology Digest of Technical Papers, June 2003, pages 135-136. V. Subramanian et al., " A Bulk-Si-Compatible Ultrathin-body SOI Technology for Sub-100m MOSFETS" Proceeding of the 57th Annual Device Research Conference, pp. 28-29 (1999) Hisamoto et al., "A Folded-channel MOSFET for Deepsub-tenth Micron Era", 1998 IEEE International Electron Device Meeting Technical Digest, pp 1032-1034 (1998)Huang et al., "Sub 50-nm FinFET: PMOS", 1999 IEEE International Electron Device Meeting Technical Digest, pp 67-70 (1999) Auth et al., "Vertical, Fully-Depleted, Surroundings Gate MOSFETS On sub-0.1um Thick Silicon Pillars", 1996 54th Annual Device Research Conference Digest, pp 108-109 (1996) Hisamoto et al., "A Fully Depleted Lean-Channel Transistor (DELTA)-A Novel Vertical Ultrathin SOI MOSFET", IEEE Electron Device Letters, V. 11(1), pp36-38 (1990). Jong-Tae Park et al., "Pi-Gate SOI MOSFET" IEEE Electron Device Letters, Vol. 22, No. 8,

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